

## Claims

What is claimed is:

1. A built-in self test circuit for testing a clock and data recovery circuit comprising:

5                    data generating means for generating a test data byte;

                  serializing means coupled to the data generating means for converting the test data byte into serial test data;

10                  clock and data recovery means coupled to the output of the serializing means for recovering the clock and test data from the serial test data;

                  deserializing means coupled to the output of the clock and data recovery means for converting the recovered serial test data into a recovered test data byte; and

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                  analyzing means connected to the output of the deserializing means for comparing the recovered test data byte to the test data byte.

20                  2. The circuit of claim 1 wherein said clock and data recovery circuit comprises a phase lock loop.

3. The circuit of claim 2 further comprising a multiplexer coupled to the clock and data recovery circuit for inputting operational serial data or said serial test data upon setting of a data selection signal (B-ENB).

5 4. The circuit of claim 2 further comprising a first multiplexer coupled to the serializing means for inputting operational data byte or said test data byte upon setting of a data selection signal (B-ENB).

10 5. The circuit of claim 4 further comprising a second multiplexer coupled to the clock and data recovery circuit for inputting operational serial data or said serial test data upon setting of a data selection signal (B-ENB).

15 6. The circuit of claim 5 wherein said test data byte is in the form of a SONET frame, and said analyzing means comprises means for detecting the start of a SONET frame.

7. The circuit of claim 6 further comprising a state machine to control said generating means and said analyzing means.

20 8. The circuit of claim 7 wherein said data generating means is a programmable data generator.

9. The circuit of claim 1 further comprising a multiplexer coupled to the serializing means for inputting operational data byte or said test data byte upon setting of a data selection signal (B-ENB).

10. The circuit of claim 1 further comprising a multiplexer coupled to the clock and data recovery circuit for inputting operational serial data or said serial test data upon setting of a data selection signal (B-ENB).

5 11. The circuit of claim 1 wherein said test data byte is in the form of a SONET frame, and said analyzing means comprises means for detecting the start of a SONET frame.

10 12. The circuit of claim 1 further comprising a state machine to control said generating means and said analyzing means.

13. The circuit of claim 1 wherein said data generating means is a programmable data generator.

14. A method for testing a clock and data recovery circuit comprising:

generating an initial test data byte;

5           inputting the test data byte to a serializer  
for conversion into serial test data;

          sending the serial test data to the clock and  
data recovery circuit for recovering the clock and  
test data from the serial test data;

10           inputting the recovered serial test data to a  
deserializer for conversion into a recovered test  
data byte; and

          comparing the recovered test data byte to the  
initial test data byte.

15           15. The method of claim 14 wherein said clock and data  
recovery circuit comprises a phase lock loop.

          16. The method of claim 15 further comprising an  
initial step of waiting for a predetermined period of time  
to allow said phase lock loop to lock to a predetermined  
frequency before beginning of said generating.

17. The method of claim 16 further comprising:

generating a new test data byte; and

repeating said serializing, recovering,  
deserializing and analyzing until the recovered  
test data byte matches the test data byte.

18. The method of claim 17 wherein said generating a  
new test data byte and said repeating are performed until a  
counter reaches a predetermined number of pulses.

19. The method of claim 18 wherein said generating and  
said analyzing are controlled by a state machine.

20. The method of claim 19 wherein said counter is  
included within said state machine.

21. The method of claim 14 further comprising an  
initial step of waiting for a predetermined period of time  
to allow said phase lock loop to lock to a predetermined  
frequency before beginning of said generating.

22. The method of claim 14 further comprising:

generating a new test data byte; and

repeating said serializing, recovering,  
deserializing and analyzing until the recovered  
test data byte matches the test data byte.

